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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,702	LIN ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *04 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,21 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,21 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-6, 12-14, 17, 21 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Shue et al., US patent No. 5,970,378.

Regarding claim 1, Shue teaches (figs. 1-5) a semiconductor device having a first layer (20c) underlying a second layer (28a, 28b), the method comprising: forming a glue layer (22a", 22b") on the first layer (20c); performing an inter-treatment (24, 26) on the glue layer (22"); wherein the inter-treatment affects the upper and lower surfaces of the glue layer and improves an adhesive interface between the glue layer and the first layer (col. 7, lines 30-42), since layer 22" is exposed to the plasma treatment the upper and lower surface of 22 are affected); and depositing the second layer (28a, 28b) directly onto the upper surface of the inter-treated glue layer (22"), wherein the inter-treated glue layer improves the adhesion between the first (20c) and the second layers (28a,28b), wherein the second layer is a metal layer (col. 7, lines 30-42).

The limitations of "a method for increasing a time dependent dielectric breakdown lifetime of a semiconductor device" is not given patentable weight because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably

distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Furthermore since Shue teaches the same claimed process, Shue's process is inherently capable of increasing a time dependent dielectric breakdown lifetime of the semiconductor device.

Regarding claim 3, Shue teaches the entire claimed process of claim 1 above including the inter-treatment on the glue layer includes applying plasma to the glue layer (col. 6, lines 15-35 and lines 44-50).

Regarding claim 4, Shue teaches the entire claimed process of claim 1 above including selecting a reacting gas, a process time, a process temperature, a process pressure, and a reacting gas flow (refer to col. 6, lines 15-65). Shue teaches performing plasma treatment on the layer using different gases at certain plasma energy. Therefore Shue's process inherently requires adjusting reacting gas flow as indicated by the chemical formal, chamber temperature and process time.

Regarding claim 5, Shue teaches the entire claimed process of claim 1 above including the selected reacting gas is a hydrogen based gas (col. 6, lines 15-20).

Regarding claim 6, Shue teaches the entire claimed process of claims 1 and 4 above including the selected reacting gas is a helium based gas (col. 6, lines 51-65).

Regarding claim 12, Shue teaches (figs. 1-5) a method comprising: depositing a dielectric layer (20c), depositing a glue layer (22") on the dielectric layer (20c); selecting

a plasma treatment process (col. 6, lines 15-65); and applying the selected treatment process to affect the upper and lower surfaces of the glue layer (col. 7, lines 33-42, since layer 22" is exposed to the plasma treatment the upper and lower surface of 22" are affected); forming a metal layer (28a, 28b) directly on the upper surface of the glue layer (22"), wherein the treatment process enhances an adhesiveness between the dielectric layer (20c) and the metal layer (28a, 28b, col. 7, lines 33-42).

The limitation of "a method for increasing a dielectric breakdown lifetime of a semiconductor device" is not given patentable weight because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Furthermore since Shue teaches the same claimed process, Shue's process is inherently capable of increasing a time dependent dielectric breakdown lifetime of the semiconductor device.

Regarding claim 13, Shue teaches the entire claimed process of claim 1 above including the glue layer (22") with a certain thickness.

The limitation "the selected thickness is based at least partially on a desired electrical property of the glue layer" is not given patentable weight because the feature does not add anything to the process of forming the glue layer. Furthermore since Shue

is concerned with forming interconnection structure therefore Shue's process is inherently concerned with finding the desired electrical property of the glue layer.

Regarding claim 14, Shue teaches the entire claimed process of claim 1 above including adjusting a property of the selected treatment process based on the selected thickness of the glue layer.

Shue teaches forming the treatment over a certain depth of the glue layer. Therefore Shue is inherently capable of adjusting a property of the selected treatment process based on the selected thickness of the glue layer.

Regarding claim 17, Shue teaches the entire claimed process of claims 1 and 12 above including the selected process is the plasma treatment process, and wherein a reacting gas to be used in the plasma treatment process is hydrogen based gas (col. 6, lines 15-20).

3. Claims 21, 23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Dixit et al., US patent No. 6,355,558.

Regarding claim 21, Dixit teaches (fig. 2C) forming a first metal layer (42); forming a glue layer (44, wetting layer, same as a glue layer, refer to col. 4, lines 45-46, states layer 44 also acts a wetting/nucleation layer for subsequent metallization) on the first metal layer (202); performing an inter-treatment on the glue layer to alter upper and lower surfaces of the glue layer for improved adhesiveness (col. 4, lines 52-62); and forming a second metal layer (46) on the upper surface of the glue layer (44) such that an interface is formed directly between metal of the metal layer and the upper surface of

the glue layer (an interface between the second metal layer and the upper surface of the glue layer is inherently formed).

The limitations of "a method for improving an interface in a semiconductor device" is not given patentable weight because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Furthermore since Dixit teaches the same claimed process, Dixit's process is inherently capable of improving an interface in a semiconductor device.

Regarding claim 23, Dixit teaches the entire claimed process of claim 21 above including the inter-treatment includes using plasma (col. 4, lines 52-62).

Regarding claim 25, Dixit teaches (fig. 2C) forming a first metal layer (42); forming a glue layer (44, wetting layer, same as a glue layer, refer to col. 4, lines 45-46, states layer 44 also acts a wetting/nucleation layer for subsequent metallization) directly on the first metal layer (42); performing an inter-treatment on the glue layer to alter upper and lower surfaces of the glue layer (col. 4, lines 52-62) for improved adhesiveness, and forming a second metal layer (46) on the upper surface of the glue layer (44).

The limitations of "a method for improving an interface in a semiconductor device" is not given patentable weight because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Furthermore since Dixit teaches the same claimed process, Dixit's process is inherently capable of improving an interface in a semiconductor device.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shue in view of Cox et al. US patent No. 5,851,927.

Shue teaches substantially the entire claimed process of claim 1 above except explicitly stating performing a pre-treatment on the first layer before forming the glue layer.

It is conventional and also taught by Cox performing a pre-treatment process on a silicon nitride film (col. 3, lines 15-32) in order to promote adhesion between the silicon nitride layer and subsequent layers.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the pretreatment process taught by Cox in the method of Shue in order to promote adhesion between the first layer and the glue layer.

6. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shue.

Regarding claim 7, Shue teaches substantially the entire claimed process of claims 1 and 4 above except explicitly stating that the selected process time is between approximately 1 and 100 seconds, the selected process temperature is between approximately 200 and 400° C, the selected process pressure is between approximately 0.5 and 10 torr, and the selected reacting gas flow is between approximately 100 and 2500 sccm.

Parameters such as process time, temperature, pressure and reacting gas flow in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired film quality during device fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made adjust the process time, temperature, pressure and flow as claimed in the process of Shue in order to form a high quality glue layer.

Regarding claim 15, Shue teaches substantially the entire claimed process of claims 1 and 14 above except explicitly stating duration of the selected treatment process.

Parameters such as process time are subject to routine experimentation and optimization to achieve the desired film quality during device fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made adjust the process time as claimed in the process of Shue in order to form a high quality glue layer.

7. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shue in view of Murokh et al. US patent No. 5,798,146.

Regarding claim 8, Shue teaches substantially the entire claimed process of claim 1 above except explicitly stating performing the inter-treatment on the glue layer includes directing an electron beam towards the glue layer.

Murokh teaches (col. 1, lines 34-46) the application of electron beam on a dielectric layer in order to improve to the wettability and adhesive characteristics.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of applying electron beam on the dielectric layer taught by Murokh in the process of Shue in order to improve the adhesive characteristics of the glue layer.

Regarding claim 9, Shue teaches substantially the entire claimed process of claims 1 and 8 above including directing the electron beam towards the glue layer further comprises defining a process power and a dosage. Since applying electron

beam requires using a certain amount of process power and electron beam density, the combined process of Shue and Murokh inherently teaches defining a process power and a dosage.

Regarding claims 10 and 11, Shue teaches substantially the entire claimed process of claims 1 and 8 above except explicitly stating that the process power is between approximately 1000 eV and 8000 eV and the dosage is between approximately 50 and 500 $\mu C/cm^2$.

Parameters such as process power and electron beam dosage in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired film quality during device fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made adjust the process power and beam dosage as claimed in the process of Shue in order to order to improve the adhesive characteristics of the glue layer.

8. Claims 16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shue in view of You et al. US patent No. 6,271,273.

Regarding claim 16, Shue teaches the entire claimed process of claims 1 and 12 above except explicitly stating that selecting a material for forming the glue layer, wherein the material is selected from the group selected from the group consisting of SiN, silicon dioxide, SiCH, SiCN, and SiCO.

You teaches the use of material such as silicon nitride, titanium nitride as adhesion layers in the process of forming vias and trenches (col. 16, lines 54-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the titanium nitride glue layer taught by Shue with silicon nitride as taught by You in order form interconnect structures.

Regarding claim 24, Shue teaches substantially the entire claimed process of claim 21 above except explicitly stating that selecting a material for forming the glue layer, wherein the material is selected from the group selected from the group consisting of SiN, silicon dioxide, SiCH, SiCN, and SiCO.

You teaches the use of material such as silicon nitride, titanium nitride as adhesion layers in the process of forming vias and trenches (col. 16, lines 54-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the titanium nitride glue layer taught by Shue with silicon nitride as taught by You in order form interconnect structures.

Response to Arguments

9. Applicant's arguments with respect to claims 1-17 and 21, and 23-24 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 10/4/2006 have been fully considered but they are not persuasive. Applicant argues the structure of Dixit et al. teaches glue layer (42) and teaches a barrier layer formed on the glue layer. However, Dixit teaches later 44 as wetting layer, same as a glue layer, (refer to col. 4, lines 45-46, states layer 44 also acts a wetting/nucleation layer for subsequent metallization) formed on layer (42). The reference by Dixit reads on the claimed invention forming (fig. 2C) a first metal layer

(42); forming a glue layer (44, wetting layer, same as a glue layer, refer to col. 4, lines 45-46, states layer 44 also acts a wetting/nucleation layer for subsequent metallization) directly on the first metal layer (42); performing an inter-treatment on the glue layer to alter upper and lower surfaces of the glue layer (col. 4, lines 52-62) for improved adhesiveness, and forming a second metal layer (46) on the upper surface of the glue layer (44).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571)-272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
December 5, 2006

Douglas W. Owens 12/9/06

DOUGLAS W. OWENS
PRIMARY EXAMINER